CLAIMS:

1. A method for coding information in an electronic circuit, said circuit comprising at least two electrically coupled signal paths characterized in that the method comprises the steps of:

determining the relative delay between signals propagating on said paths when said signals make a transition from a first logic level to a second logic level; and

producing an output signal having a further logic level depending on the relative delay between said signals.

2. The method according to claim 1, further comprising the step of:

dividing a logical signal into two signals to be propagated on a respective one of said signal paths.

3. The method according to claim 1 or 2, further comprising the step of:

creating a reference signal being synchronized with the fastest signal propagating on either of said signal paths.

4. The method according to any of the preceding claims, further comprising the step of:

creating a relative delay between the signals propagating on said signal paths.

5. The method according to claim 1, wherein the producing step is performed by means of a delay decoder.

6. An electronic circuit for coding information, said circuit comprising at least two electrically coupled signal paths characterized in that the circuit comprises:

means for determining the relative delay between signals propagating on said paths when said signals make a transition from a first logic level to a second logic level; and

means for producing an output signal having a further logic level depending on the relative delay between said two signals.

7. The circuit according to claim 6, further comprising:

means for dividing a logical signal into two signals to be propagated on a respective one of said signal paths.

8. The circuit according to claim 6 or 7, further comprising:

means for creating a reference signal (Φ) being synchronized with the fastest signal propagating on either of said signal paths.

9. The circuit according to claim 6, further comprising:

means for creating a relative delay between the signals propagating on said signal paths.

10. The circuit according to any of claims 6, wherein the producing means comprise a delay decoder.